C L A I M S

1. A semiconductor device characterized by comprising:

a first conductivity type semiconductor substrate;

a vertical power MOSFET that employs the first conductivity type semiconductor substrate as a first conductivity type drain layer; and

a separating member formed on the first conductivity type semiconductor substrate, separating the power MOSFET from other element,

the power MOSFET characterized by comprising:

a semiconductor structure comprising three semiconductor layers selectively formed on a main surface of the first conductivity type semiconductor substrate, the three semiconductor layers including a second conductivity type semiconductor layer and two first conductivity type semiconductor layers formed to interpose the second conductivity type semiconductor layer from both side surfaces, a pn junction boundary between the second conductivity type semiconductor layer and the first conductivity type semiconductor layer being substantially vertical to the main surface of the first conductivity type semiconductor substrate,

a second conductivity type base layer formed on an upper surface of the second conductivity type semiconductor layer and having an impurity concentration higher than the second conductivity type

semiconductor layer;

a first conductivity type source diffusion layer selectively formed on a surface of the second conductivity type base layer;

a gate insulating film formed on the second conductivity type base layer interposed between the first conductivity type source diffusion layer and the first conductivity type semiconductor layer, and

a gate electrode formed on the gate insulating film.

2. The semiconductor device according to claim 1, characterized in that a concentration of a first conductivity type impurity in the first conductivity type semiconductor layer is 3 to 18 $\times 10^{15}$ (atoms/cm^3) and a concentration of a second conductivity type impurity in the second conductivity type semiconductor layer is 0.2 to 8 $\times 10^{15}$ (atoms/cm^3).

3. The semiconductor device according to claim 1, characterized in that the first conductivity type impurity in the first conductivity type semiconductor layer is arsenic and the second conductivity type impurity in the second conductivity type semiconductor layer is boron.

4. The semiconductor device according to claim 1, characterized in that an inequality: $100 \times |A - B| / A \leqq 5$ is satisfied where A represents a total amount of a second conductivity type impurity in the second

conductivity type semiconductor layer and B represents a total amount of a first conductivity type impurity in the two first conductivity type semiconductor layers.

5. The semiconductor device according to claim 1, characterized in that a first conductivity type diffusion layer having an impurity concentration higher than the first conductivity type semiconductor layer is formed on an upper surface of the first conductivity type semiconductor layer.

6. The semiconductor device according to claim 5, characterized in that the concentration of a first conductivity type impurity in the first conductivity type diffusion layer is substantially the same as a first conductivity type impurity in the first conductivity type source diffusion layer.

7. The semiconductor device according to claim 1, characterized in that the separating member includes a semiconductor layer formed above the first conductivity type semiconductor substrate, and an insulating film formed to cover a bottom surface, side surfaces and an upper surface of the semiconductor layer.

8. The semiconductor device according to claim 1, characterized in that the separating member includes a semiconductor layer formed above the first conductivity type semiconductor substrate, and an insulating film formed to cover a bottom surface and side surfaces of the semiconductor layer.

9. The semiconductor device according to any one of claims 1 to 8,characterized in that a plurality of power MOSFETs identical to the power MOSFET are formed such as to employ the first conductivity type semiconductor substrate as a common first conductivity type drain layer and

a termination structure is provided in which one of the first conductivity type and second conductivity type semiconductor layers on a terminal portion of the first conductivity type semiconductor substrate is connected to a power MOSFET that is closest to the terminal portion via an insulating film formed on the first conductivity type semiconductor substrate.

10. The semiconductor device according to any one of claims 1 to 8, characterized in that a plurality of power MOSFETs identical to the power MOSFET are formed such as to employ the first conductivity type semiconductor substrate as a common first conductivity type drain layer, and a corner portion of an element region containing the power MOSFETs is formed into a round or polygonal shape.

11. The semiconductor device according to claim 10, characterized in that a corner portion of the separating member located adjacent to the element region is formed into a round or polygonal shape.

12. The semiconductor device according to any one of claims 1 to 8, characterized in that a plurality of

power MOSFETs identical to the power MOSFET are formed such as to employ the first conductivity type semiconductor substrate as a common first conductivity type drain layer,

a first gate wiring for the gate electrodes of the power MOSFETs are provided in a peripheral portion of an element region that contains the power MOSFETs, and

a second gate wiring for the gate electrodes of the power MOSFETs, which extend from the peripheral portion of the element region towards an inside of the element region, are connected to the first gate wiring.

13. The semiconductor device according to claim 12, characterized in that the power MOSFETs are absent in the element region located underneath the second gate wiring.

14. The semiconductor device according to claim 13, characterized in that the semiconductor structure that is physically separated from the power MOSFET by the separating member, is formed in the element region located underneath the second gate wiring.

15. The semiconductor device according to any one of claims 1 to 8, characterized in that a plurality of power MOSFETs identical to the power MOSFET are formed such as to employ the first conductivity type semiconductor substrate as a common first conductivity type drain layer,

a termination region for the element region that contains the power MOSFETs is separated from the element region by the separating member,

the first conductivity type semiconductor layer and the second conductivity type semiconductor layer are further formed in line on a side surface of the separating member on the termination region side;

a source electrode is formed such as to be in contact with each of the first conductivity type source diffusion layers of the power MOSFETs; and

an end portion of the source electrode on the termination region side extends 10 μm or more than an end portion on the termination region side of the first conductivity type semiconductor layer further formed on the side surface of the separating member on the termination region side is set to 10 μm or more.

16. The semiconductor device according to claim 15, characterized in that a gate wiring structure is formed on the termination region.

17. A method of manufacturing a semiconductor device, characterized by comprising:

growing a first conductivity type epitaxial semiconductor layer having a low impurity concentration on a first conductivity type semiconductor substrate having a high impurity concentration;

making a plurality of trenches in the first conductivity type epitaxial semiconductor layer so as

to reach the first conductivity type semiconductor substrate;

implanting a first conductivity type impurity and a second conductivity impurity having a diffusion coefficient larger than the first conductivity type impurity to side surfaces of the trenches by an ion implantation method, thereby converting the first conductivity type epitaxial semiconductor layer in a region interposed between the trenches into a semiconductor structure comprising a second conductivity type semiconductor layer and two first conductivity type semiconductor layers formed to sandwich the second conductivity type semiconductor layer from both side surfaces by using a difference between the impurities in diffusion coefficient, a pn junction boundary between the second conductivity type semiconductor layer and the first conductivity type semiconductor layer being substantially vertical to the main surface of the first conductivity type semiconductor substrate;

forming a first insulating film on at least a bottom surface and side surfaces of the trenches;

forming a second conductivity type base layer having an impurity concentration higher than the second conductivity type semiconductor layer on an upper surface of the second conductivity type semiconductor layer;

selectively forming a first conductivity type source diffusion layer on a surface of the second conductivity type base layer; and

forming a gate insulating film and a gate electrode on the second conductivity type base layer interposed between the first conductivity type source diffusion layer and the first conductivity type semiconductor layer.

18. The method of manufacturing a semiconductor device according to claim 17, characterized in that arsenic is used as the first conductivity type impurity and boron is used as the second conductivity type impurity.

19. The method of manufacturing a semiconductor device according to claim 17, a concentration of a first conductivity type impurity in the first conductivity type epitaxial semiconductor layers is set to 5×10^{13} to 3×10^{14} (atoms/cm^3), a concentration of the first conductivity type impurity in the first conductivity type semiconductor layer is set to 3 to 18×10^{15} (atoms/cm^3), and a concentration of a second conductivity type impurity in the second conductivity semiconductor layer is set to 0.2 to 8×10^{15} (atoms/cm^3).

20. The method of manufacturing a semiconductor device according to claim 17, characterized in that the trench is filled with a semiconductor layer via the

first insulating film.

21. The method of manufacturing a semiconductor device according to claim 20, characterized in that after a second insulating film made of a material different from the first insulating film is formed on a surface of the first conductivity type epitaxial semiconductor layer, the second insulating film and the first conductivity type epitaxial semiconductor layers are etched such as to make the trench, followed by forming the first insulating film, thereby growing the semiconductor layer inside the trench on a priority basis.

22. The method of manufacturing a semiconductor device according to claim 17, characterized in that the trench is filled to a depth half way through of the trench with the semiconductor layer via the first insulating film, and then an unfilled portion of the trench is filled with a third insulating film.